

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

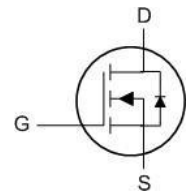
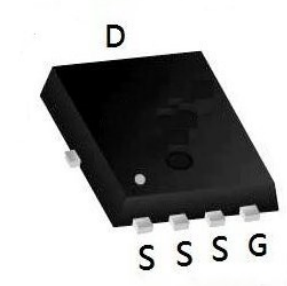
Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

Product Summary

BVDSS	$R_{DS(ON)}$	ID
60V	6.5m Ω	65A

PDFN5060-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	65	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	40	A
I_{DM}	Pulsed Drain Current ²	260	A
EAS	Single Pulse Avalanche Energy ³	57.8	mJ
I_{AS}	Avalanche Current	17	A
$P_D @ T_C = 25^\circ\text{C}$	Total Power Dissipation ⁴	31.25	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	52	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	4	$^\circ\text{C/W}$

Typical Characteristics

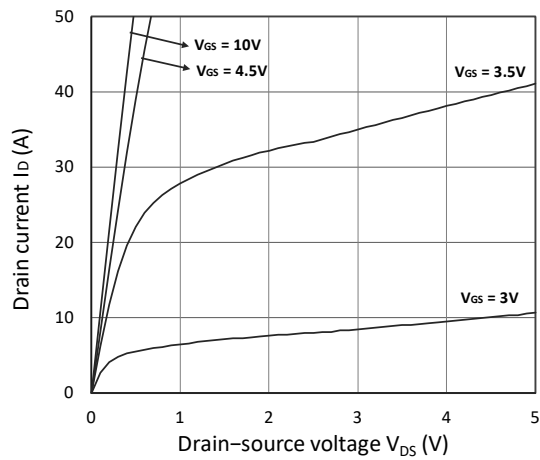


Figure 1. Output Characteristics

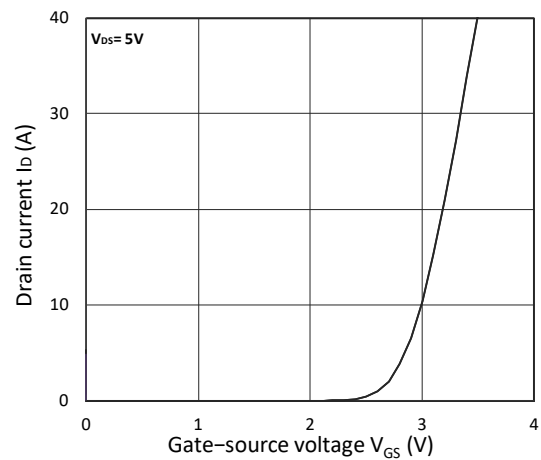


Figure 2. Transfer Characteristics

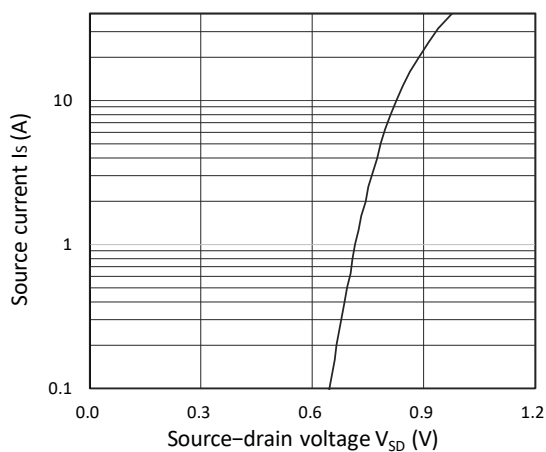


Figure 3. Forward Characteristics of Reverse

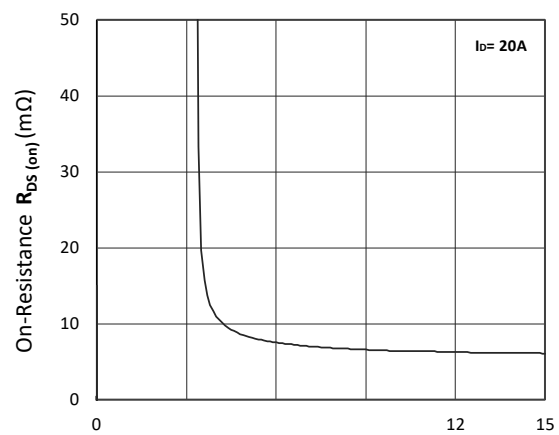


Figure 4. $R_{DS(on)}$ vs. V_{GS}

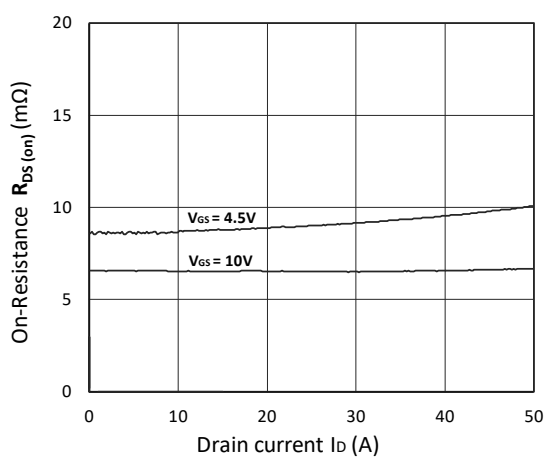


Figure 5. $R_{DS(on)}$ vs. I_D

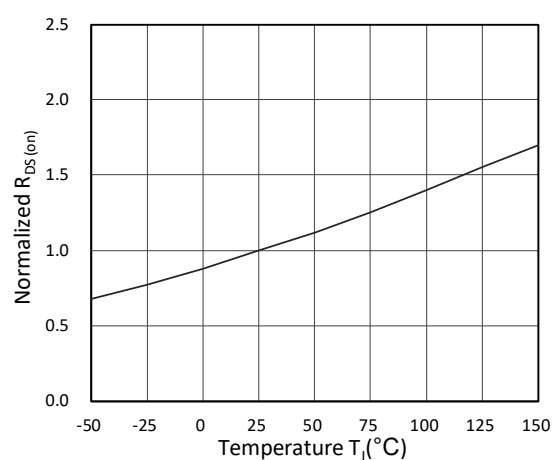


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

60V N-Channel Enhancement Mode MOSFET

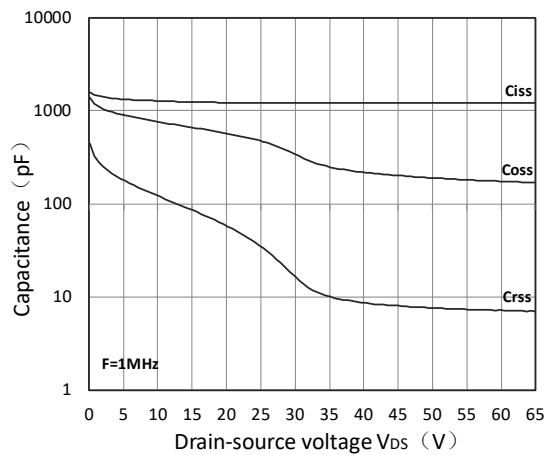


Figure 7. Capacitance Characteristics

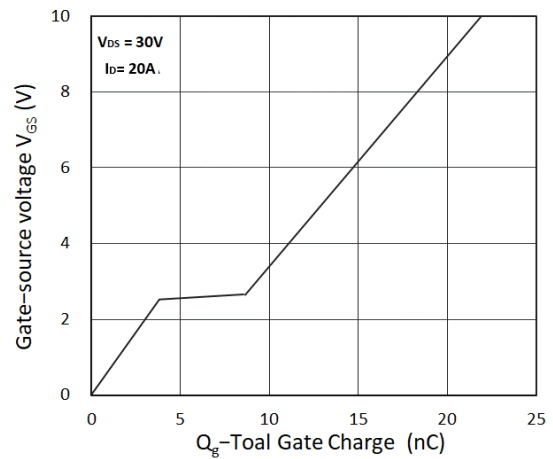


Figure 8. Gate Charge Characteristics

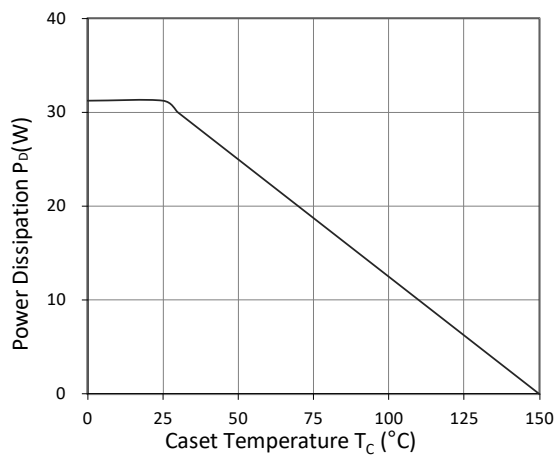


Figure 9. Power Dissipation

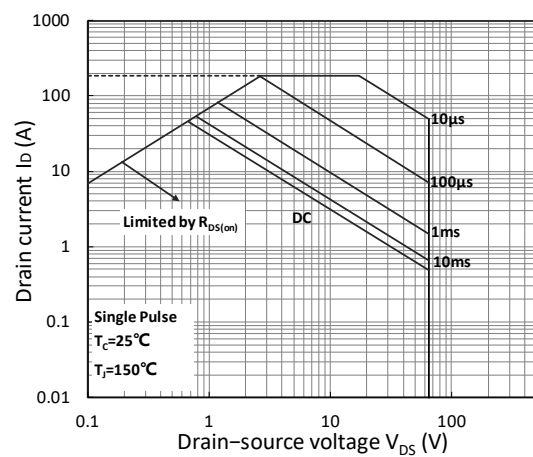


Figure 10. Safe Operating Area

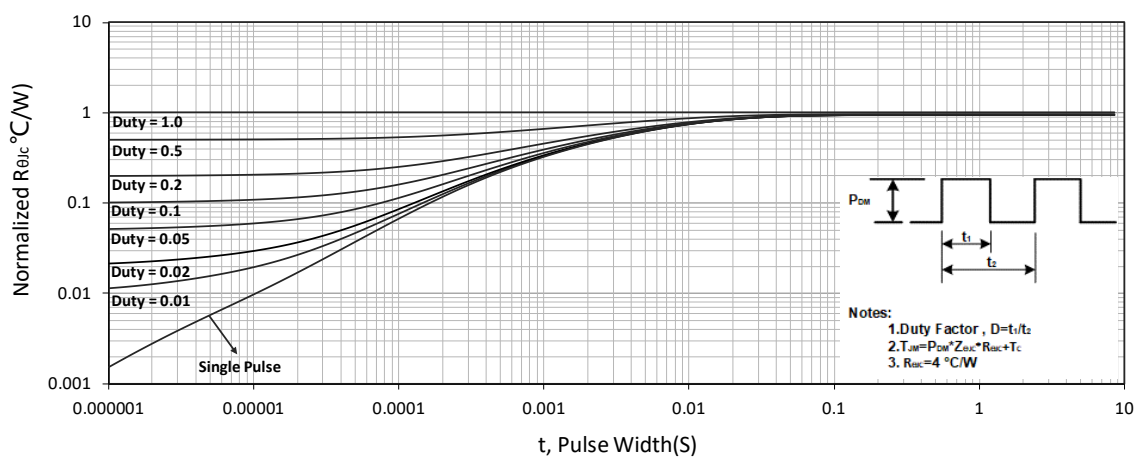
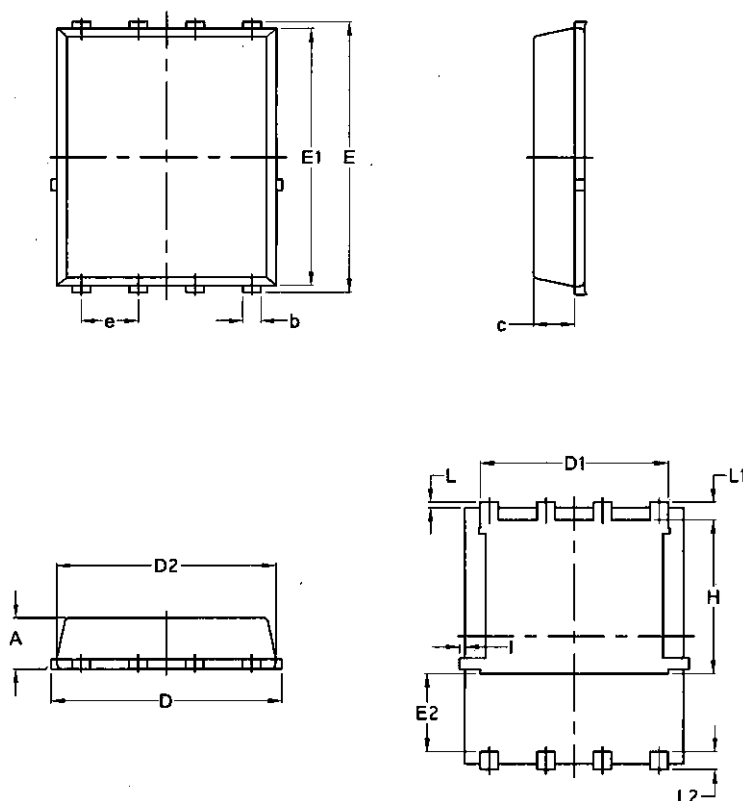


Figure 11. Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-PDFN5060-8L-JQ Single


Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

60V N-Channel Enhancement Mode MOSFET

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C \pm 5°C	5sec \pm 1 sec
Pb-Free device	260°C \pm 0/-5°C	5sec \pm 1 sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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