-100V P-Channe Enhancement Mode Power MOSFET

RoHS COMPLIANT

Description

The XPX90P10RD uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

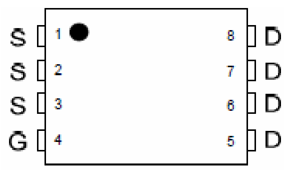
V_{DS} =-100V, I_D =-90A
RDS(ON)=11mΩ@VGS=-10V
RDS(ON)=14mΩ@VGS=-4.5V

General Features

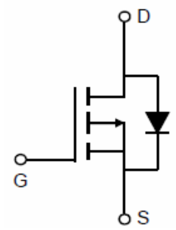
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Load switch
- Battery protection

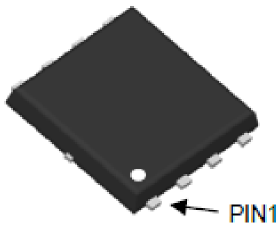


Pin Assignment

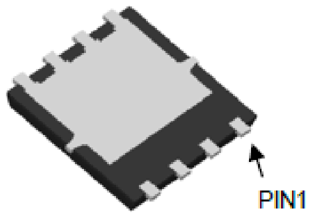


Schematic diagram

Top View



Bottom View



Product ID	Pack	Marking	Qty(PCS)
XPX90P10RD	PDFN5X6-8L	XPX90P10RD XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-95	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25˚C	Continuous Drain Current, V_{GS} @ -10V[1]	-100	A
I_D@T_C=100˚C	Continuous Drain Current, V_{GS} @ -10V[1]	-66	A
I_{DM}	Pulsed Drain Current[2]	-300	A
EAS	Single Pulse Avalanche Energy[3]	174	mJ
I_{AS}	Avalanche Current	-50	A
P_D@T_C=25˚C	Total Power Dissipation[4]	280	W
T_{STG}	Storage Temperature Range	-55 to 150	˚C
T_J	Operating Junction Temperature Range	-55 to 150	˚C
$R_{θJA}$	Thermal Resistance Junction-Ambient [1]	25	˚C/W
$R_{θJC}$	Thermal Resistance Junction-Case[1]	1.1	˚C/W

Electrical Characteristics (TJ =25 ℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-95	-102	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=-95V, V_{GS}=0V,	-	-	-1.0	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}= ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1.0	-1.6	-2.5	V
RDS(on)	Static Drain-Source on-Resistance	V_{GS}=-10V, I_D=-20A	-	11	16	mΩ
		V_{GS}=-4.5V, I_D=-10A	-	14	20	
Ciss	Input Capacitance	V_{DS}=-50V, V_{GS}=0V, f=1.0MHz	-	4100	-	pF
Coss	Output Capacitance		-	900	-	pF
Crss	Reverse Transfer Capacitance		-	55	-	pF
Q_g	Total Gate Charge	V_{DS}=-50V, I_D=-20A, V_{GS}=-10V	-	58	-	nC
Qgs	Gate-Source Charge		-	12.9	-	nC
Qgd	Gate-Drain(“Miller”) Charge		-	10.2	-	nC
td(on)	Turn-on Delay Time	V_{DD}=-50V, I_D=-5A, R_G=6Ω, V_{GS}=-10V	-	15	-	ns
tr	Turn-on Rise Time		-	17	-	ns
td(off)	Turn-off Delay Time		-	70	-	ns
t_f	Turn-off Fall Time		-	15	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-100	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-300	A
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S=-6.2A	-	-	-1.2	V
trr	Body Diode Reverse Recovery Time	T_J=25℃, I_F=-10A,dI/dt=100A/μs	-	42	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	20	-	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3、The EAS data shows Max. rating . The test condition is VDD =-72V,VGS =-10V,L=0.1mH,IAS =-50A
4、The power dissipation is limited by 150℃ junction temperature
5、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

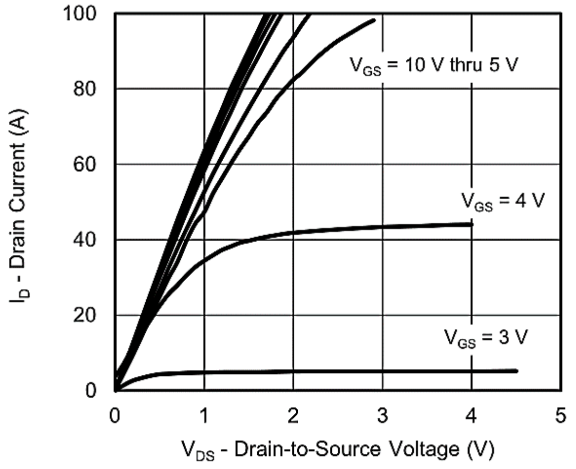


Figure 1:Output Characteristics

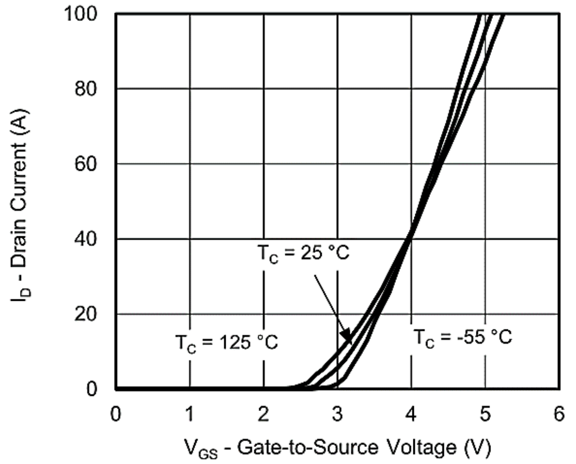


Figure 2:Transfer Characteristics

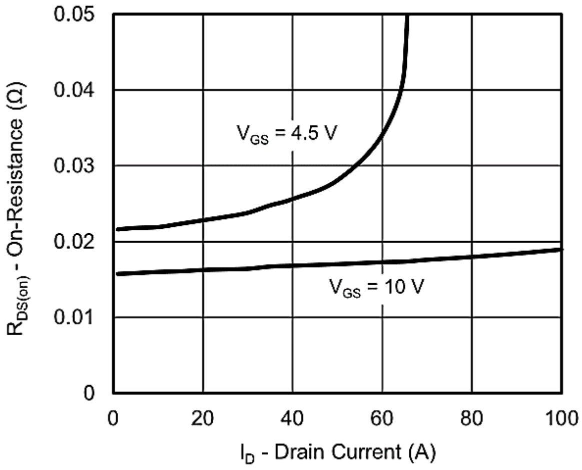


Figure 3:On-Resistance vs. Drain Current

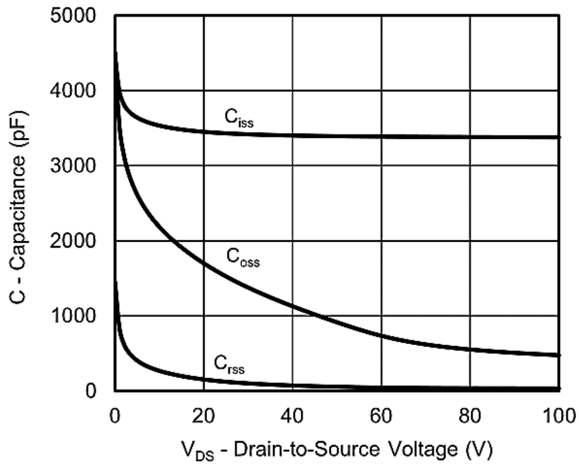


Figure 4:Capacitance

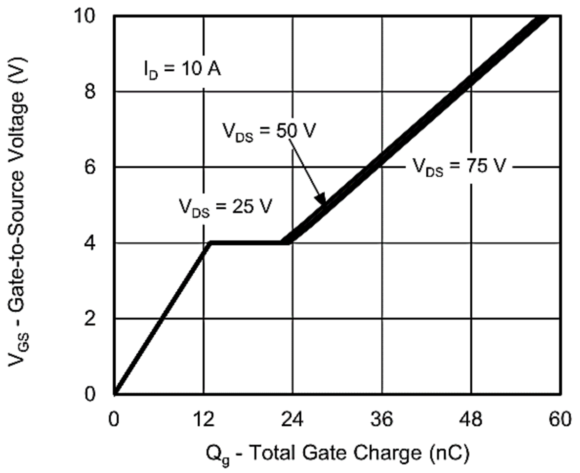


Figure 5:Gate Charge

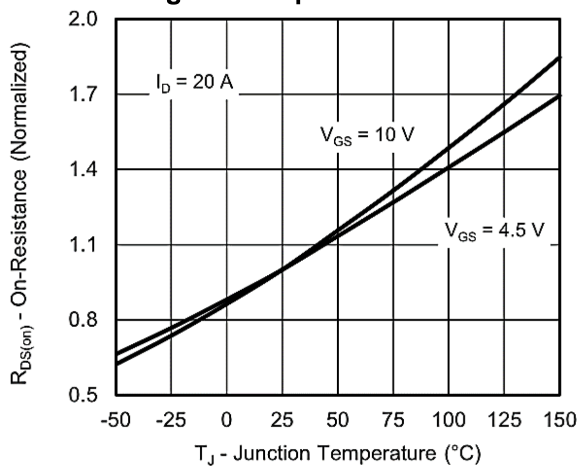


Figure 6:On-Resistance vs. Junction Temperature

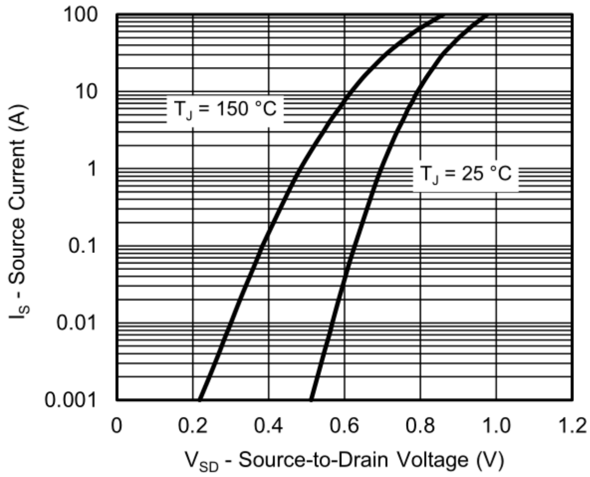


Figure 6:Source-Drain Diode Forward Voltage

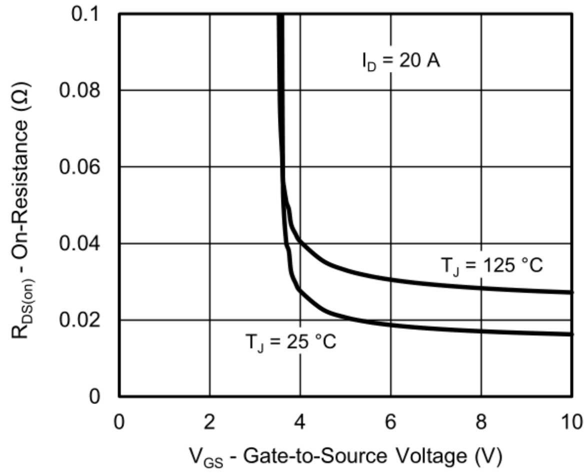


Figure 7:On-Resistance vs. Gate-to-Source Voltage

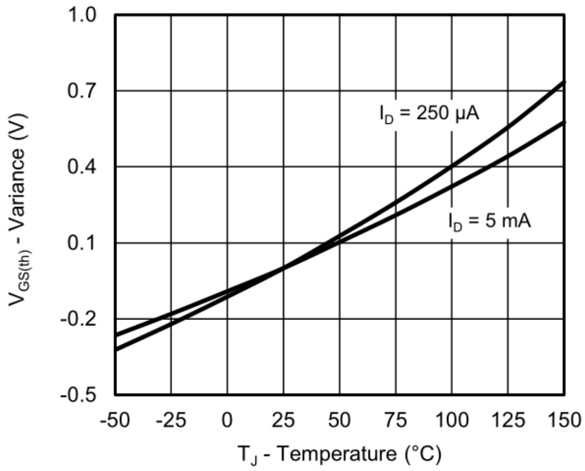


Figure 8:Threshold Voltage

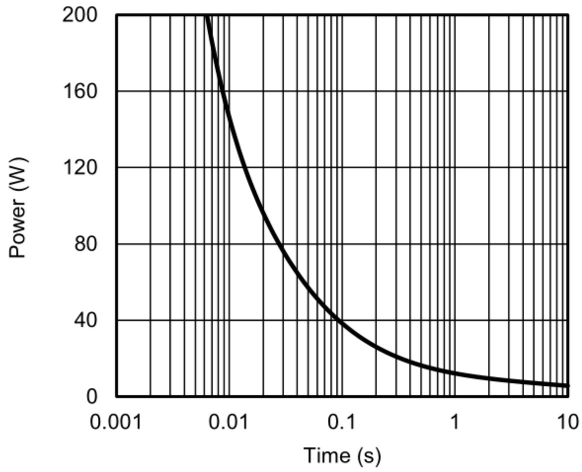


Figure9:Single Pulse Power, Junction-to-Ambient

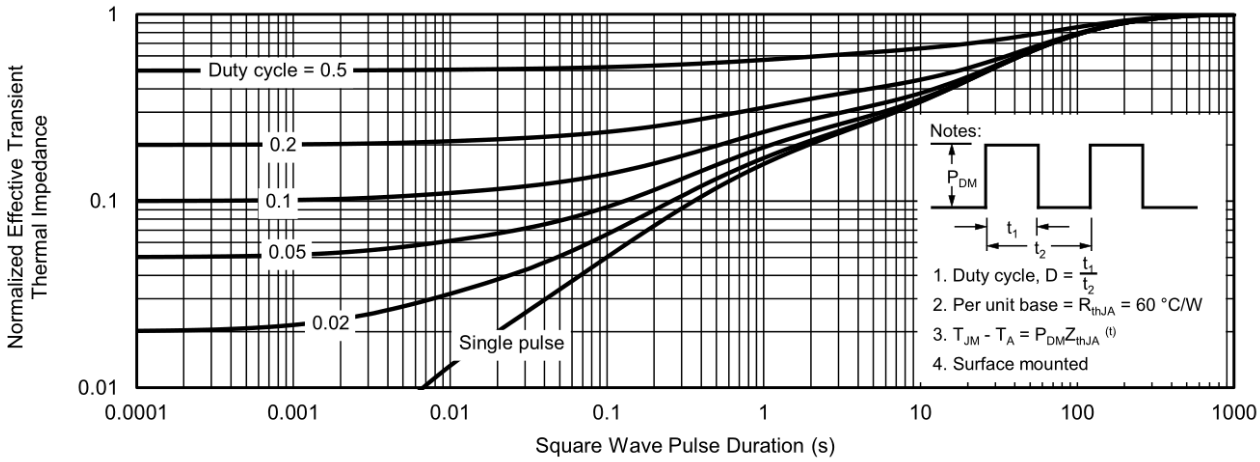
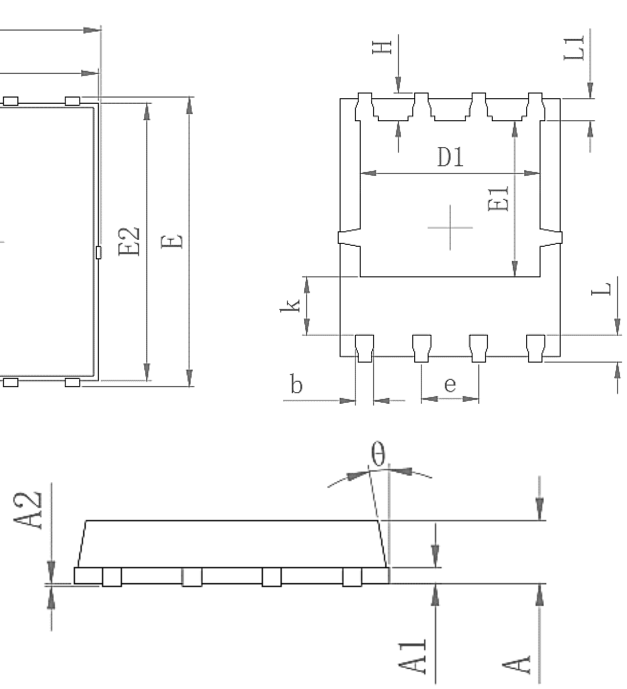


Figure11:Normalized Thermal Transient Impedance, Junction-to-Ambient

Package Mechanical Data-PDFN5X6-8L-XZT Single



Symbol	Common	
	mm	
	Mim	Max
A	0.90	1.10
A1	0.254 REF	
A2	0-0.05	
D	4.824	4.976
D1	3.910	4.110
D2	4.944	5.076
E	5.924	6.076
E1	3.375	3.575
E2	5.674	5.826
b	0.350	0.450
e	1.270	
L	0.534	0.686
L1	0.424	0.576
K	1.190	1.390
H	0.549	0.701
Φ	8°	12°

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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