

- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary

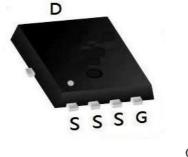


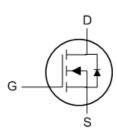
BVDSS	RDSON	ID
20V	2.2mΩ	100A

Description

The XPX100N02RD is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The XPX100N02RD meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

PDFN5060-8L Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	20	V
V _G s	Gate-Source Voltage	±12	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	100	Α
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	63	А
I _{DM}	Pulsed Drain Current ²	400	А
EAS	Single Pulse Avalanche Energy ³	306	mJ
las	Avalanche Current		А
P _D @T _C =25°C	Total Power Dissipation ⁴	69	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Тур.	Max.	Unit
Reja	Thermal Resistance Junction-Ambient ¹			°C/W
Rejc	Thermal Resistance Junction-Case ¹		1.8	°C/W



Electrical Characteristics (T_J=25 C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	20			V
△BV _{DSS} /△T _J	BV _{DSS} Temperature Coefficient	Reference to 25°C , I _D =1mA				V/ C
		V _{GS} =10V , I _D =17.5A				
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =4.5V , I _D =17.5A		2.2	2.9	mΩ
		V _{GS} =2.5V , I _D =13A		2.7	3.5	
V _{GS(th)}	Gate Threshold Voltage	V -V 1 -2500A	0.5		1	V
$\triangle V_{GS(th)}$	V _{GS(th)} Temperature Coefficient	$V_{GS}=V_{DS}$, $I_D=250uA$				mV/ C
	Drain Source Leakage Current	V _{DS} =20V , V _{GS} =0V , T _J =25°C			1	uA
I _{DSS}	Drain-Source Leakage Current	V _{DS} =20V, V _{GS} =0V , T _J =125°C			100	
Igss	Gate-Source Leakage Current	V _{GS} =±12V , V _{DS} =0V			±100	nA
gfs	Forward Transconductance	V _{DS} =5V , I _D =17.5A		88		S
Qg	Total Gate Charge			70		
Qgs	Gate-Source Charge	V _{DS} =10V , V _{GS} =4.5V , I _D =17.5A		10		nC
Q _{gd}	Gate-Drain Charge			14		
T _{d(on)}	Turn-On Delay Time			8		
Tr	Rise Time	V _{DS} =10V ,V _{GS} =4.5V ,		20		
T _{d(off)}	Turn-Off Delay Time	$R_G=3\Omega$, $R_L=0.5\Omega$		75		ns
Tf	Fall Time			82		
Ciss	Input Capacitance			5670		
Coss	Output Capacitance	V _{DS} =10V , V _{GS} =0V , f=1MHz		460		pF
C _{rss}	Reverse Transfer Capacitance			416		

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
ls	Continuous Source Current ^{1,4}	V _G =V _D =0V , Force Current			100	Α
Vsp	Diode Forward Voltage ²	V _{GS} =0V , I _S =21A , T _J =250			1	V
t _{rr}	Reverse Recovery Time	IF=17.5A , di/dt=100A/μs ,		15		nS
Qrr	Reverse Recovery Charge	T _J =250		6		nC

Note:

- 1..Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2.EAS condition: TJ=25 $^{\circ}$ C,VDD=10V,VG=10V, Rg=25 Ω , L=0.5mH.
- 3.Repetitive Rating: Pulse width limited by maximum junction temperature.e.



Typical Electrical And Thermal Characteristics (Curves)

Figure 1. Output Characteristics

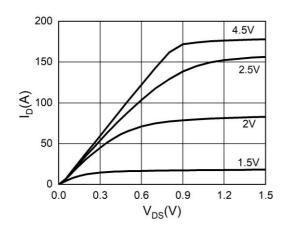


Figure 2. Transfer Characteristics

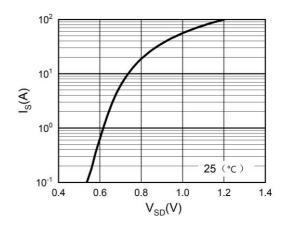


Figure 3. Power Dissipation

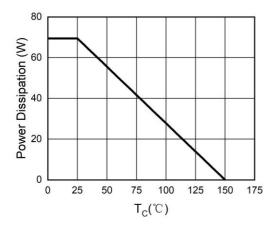


Figure 4. Drain Current

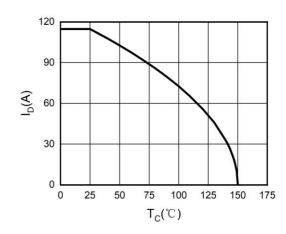


Figure 5. BV_{DSS} vs Junction Temperature

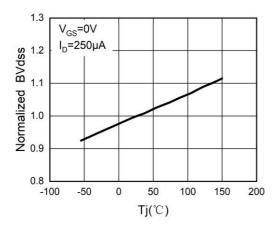
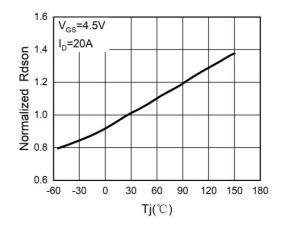


Figure 6. RDS(ON) vs Junction Temperature





Typical Electrical And Thermal Characteristics (Curves)

Figure 7. Gate Charge Waveforms

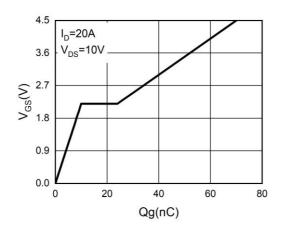


Figure 8. Capacitance

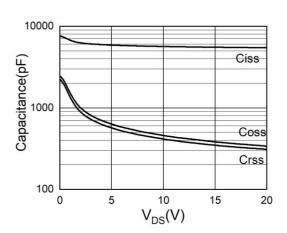


Figure 9. Body-Diode Characteristics

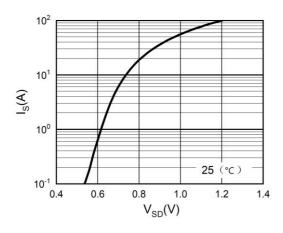
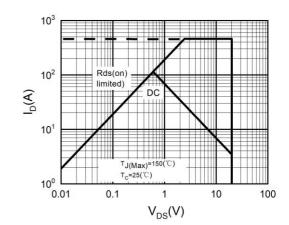
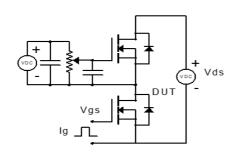


Figure 10. Maximum Safe Operating Area





Test Circuit



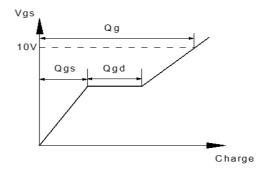
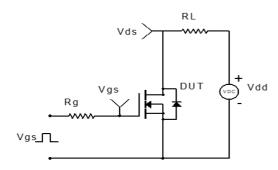


Figure 1: Gate Charge Test Circuit & Waveform



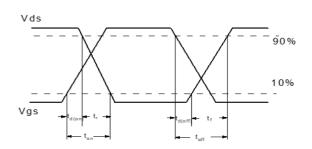
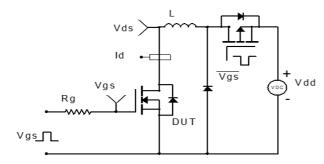


Figure 2: Resistive Switching Test Circuit & Waveform



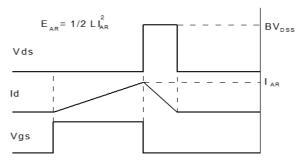
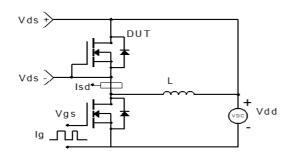


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform



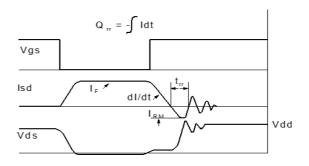
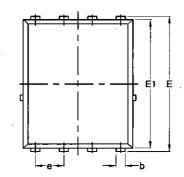
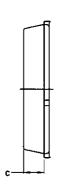


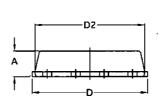
Figure 4: Diode Recovery Test Circuit & Waveform

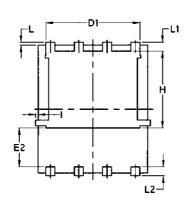


Package Mechanical Data-PDFN5060-8L-Single









Symbol	Common	Common				
	mm	mm				
	Mim	Max	Min	Max		
Α	1.03	1.17	0.0406	0.0461		
b	0.34	0.48	0.0134	0.0189		
С	0.824	0.0970	0.0324	0.082		
D	4.80	5.40	0.1890	0.2126		
D1	4.11	4.31	0.1618	0.1697		
D2	4.80	5.00	0.1890	0.1969		
E	5.95	6.15	0.2343	0.2421		
E1	5.65	5.85	0.2224	0.2303		
E2	1.60	/	0.0630	/		
е	1.27 BSC	1.27 BSC				
L	0.05	0.25	0.0020	0.0098		
L1	0.38	0.50	0.0150	0.0197		
L2	0.38	0.50	0.0150	0.0197		
Н	3.30	3.50	0.1299	0.1378		
1	/	0.18	/	0.0070		



Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec



This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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